CONFIGURATION OF THE ATLAS TRIGGER SYSTEM

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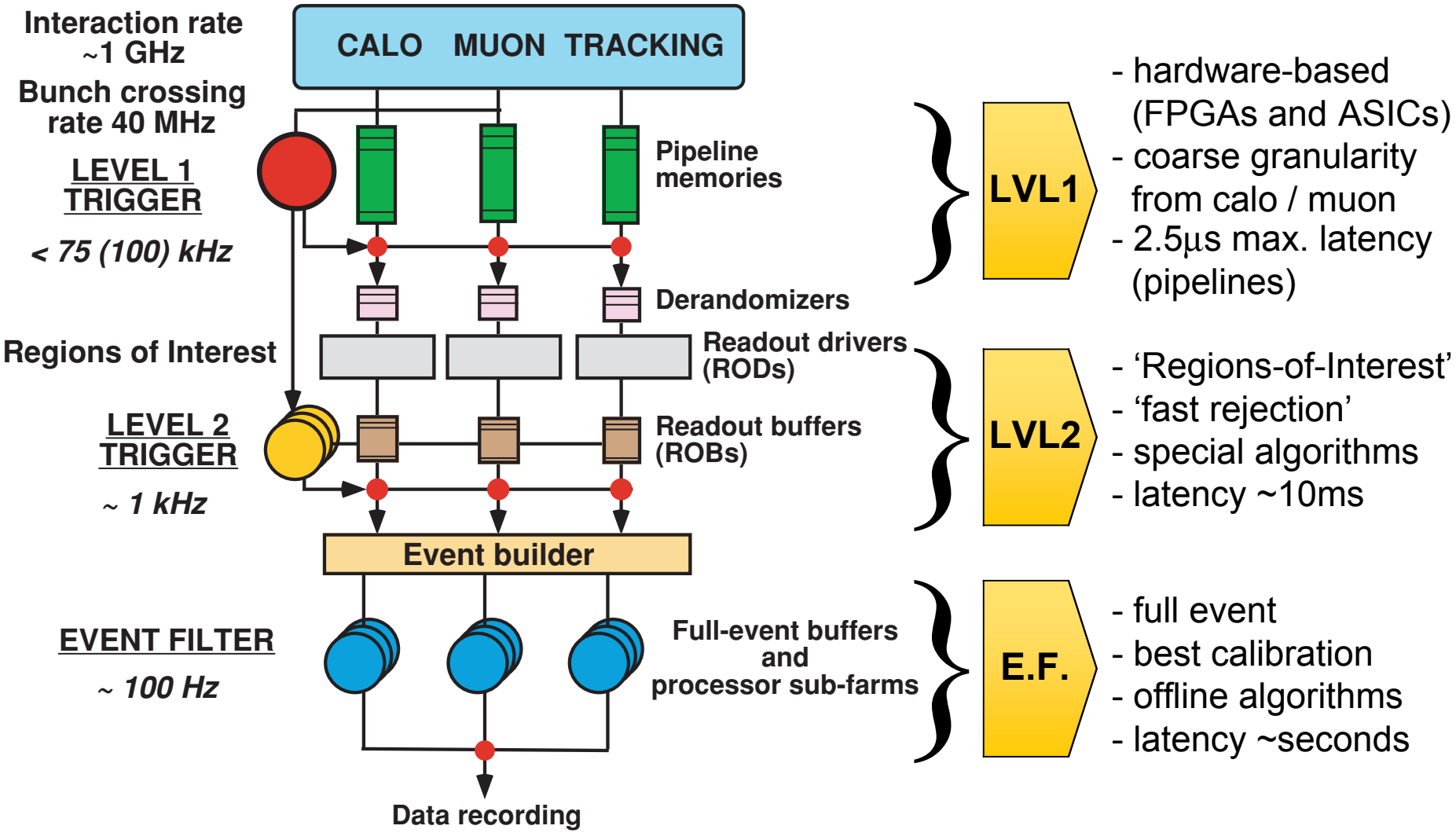
THE ATLAS TRIGGER: OVERVIEW

Multi-layer structure for rate reduction: 40 MHz (x 1.6MB) → ~100 Hz



TRIGGER CONFIGURATION

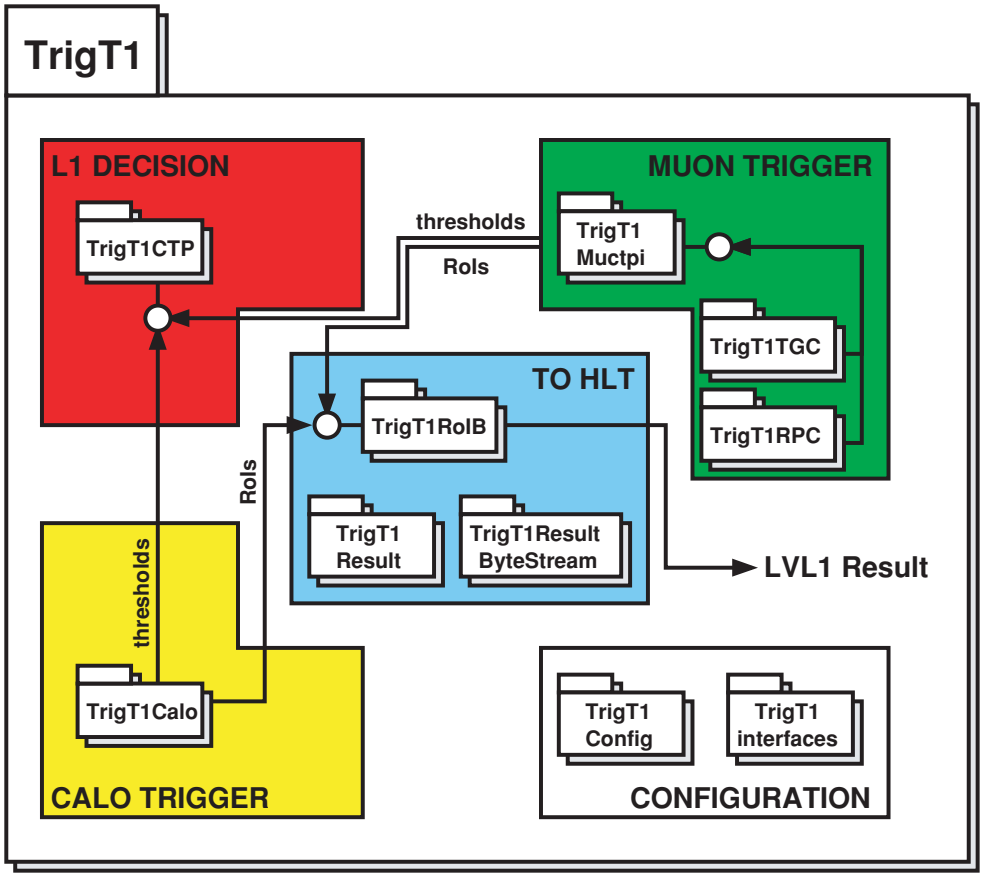
Separate efforts: LVL1 and HLT

LVL1 Configuration

- Defines LVL1 selection strategy
- Software emulation
- Hardware configuration (future)

Project:

Overall configuration of Atlas trigger

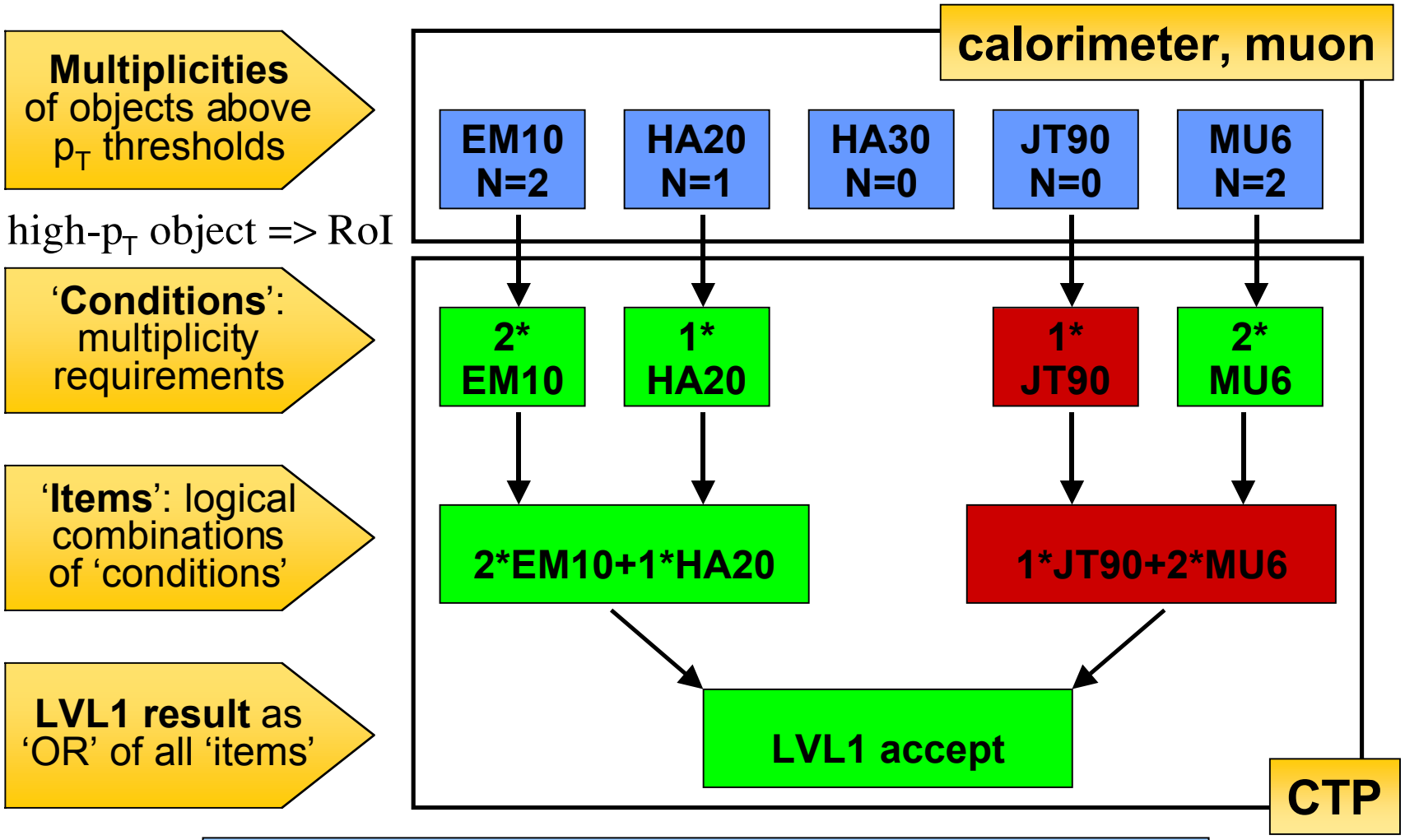


HLT Configuration

- Defines HLT selection strategy
- Algorithm sequencing setup
- LVL1 RoI seeding setup

LVL1 SELECTION STRATEGY

Based on high-p_T objects. Derive decision in CTP



Tasks: Setting up logical structure of decision

LVL1 CONFIGURATION

Based on XML, C++ and Atlas offline framework Athena :
XML parsed to C++ objects - 'remember' logical structure

Trigger Menu:
Definition of objects to be triggered

```
<TriggerMenu>
  <TriggerItem>
    <AND>
      <TriggerCondition threshold="MU6" multiplicity="2" />
      <TriggerCondition threshold="JT90" multiplicity="1" />
    </AND>
  </TriggerItem>
</TriggerMenu>
```

Logical Structure of LVL1 decision

Trigger Thresholds:
Objects for which calo and muon deliver multiplicities

```
<TriggerThreshold name="MU6"
  value="6" bitstart="3" bitlength="3" etamin="-5"  …. />
<TriggerThreshold name="JT90"
  value="90" bitstart="6" bitleng
```

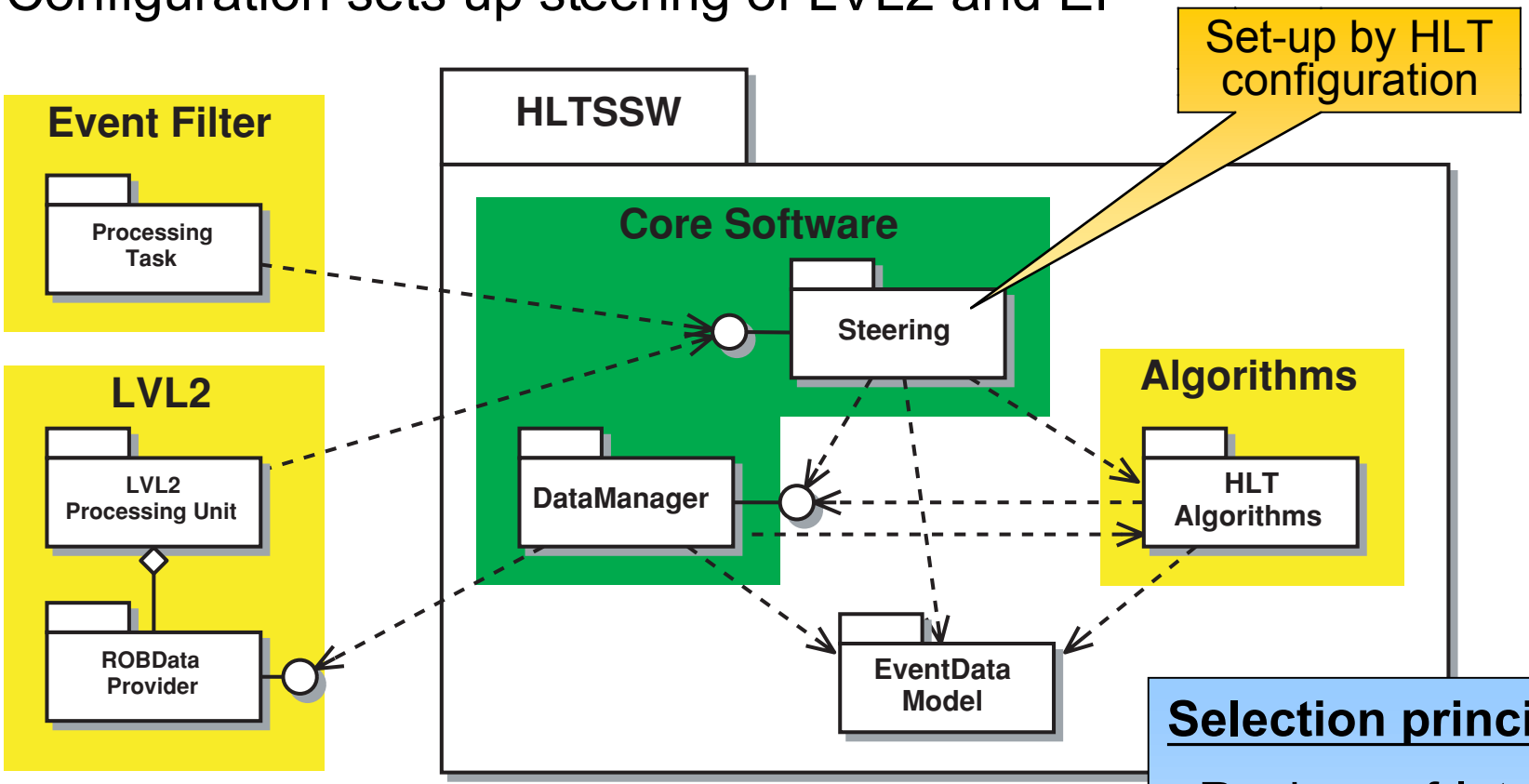
which multiplicity is to be delivered on which cable ?

Description of hardware

Prevent from configuring logical structure that exceeds CTP's abilities (number of inputs etc.).

HLT: SELECTION SOFTWARE

Configuration sets up steering of LVL2 and EF

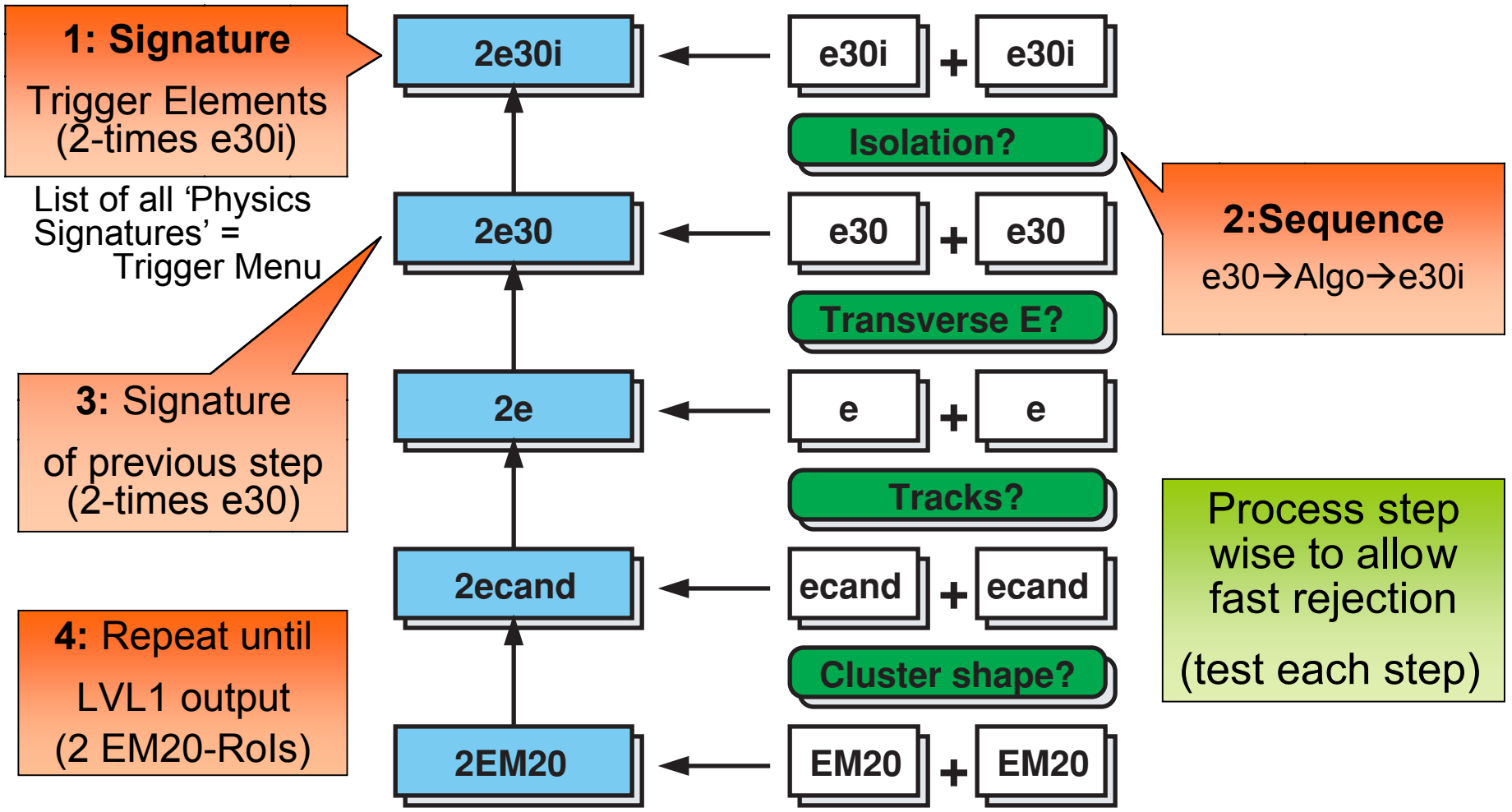


Selection principles

- Regions-of-Interest
- Fast rejection (step-wise process)
- Keep LVL2 / E.F. boundary flexible

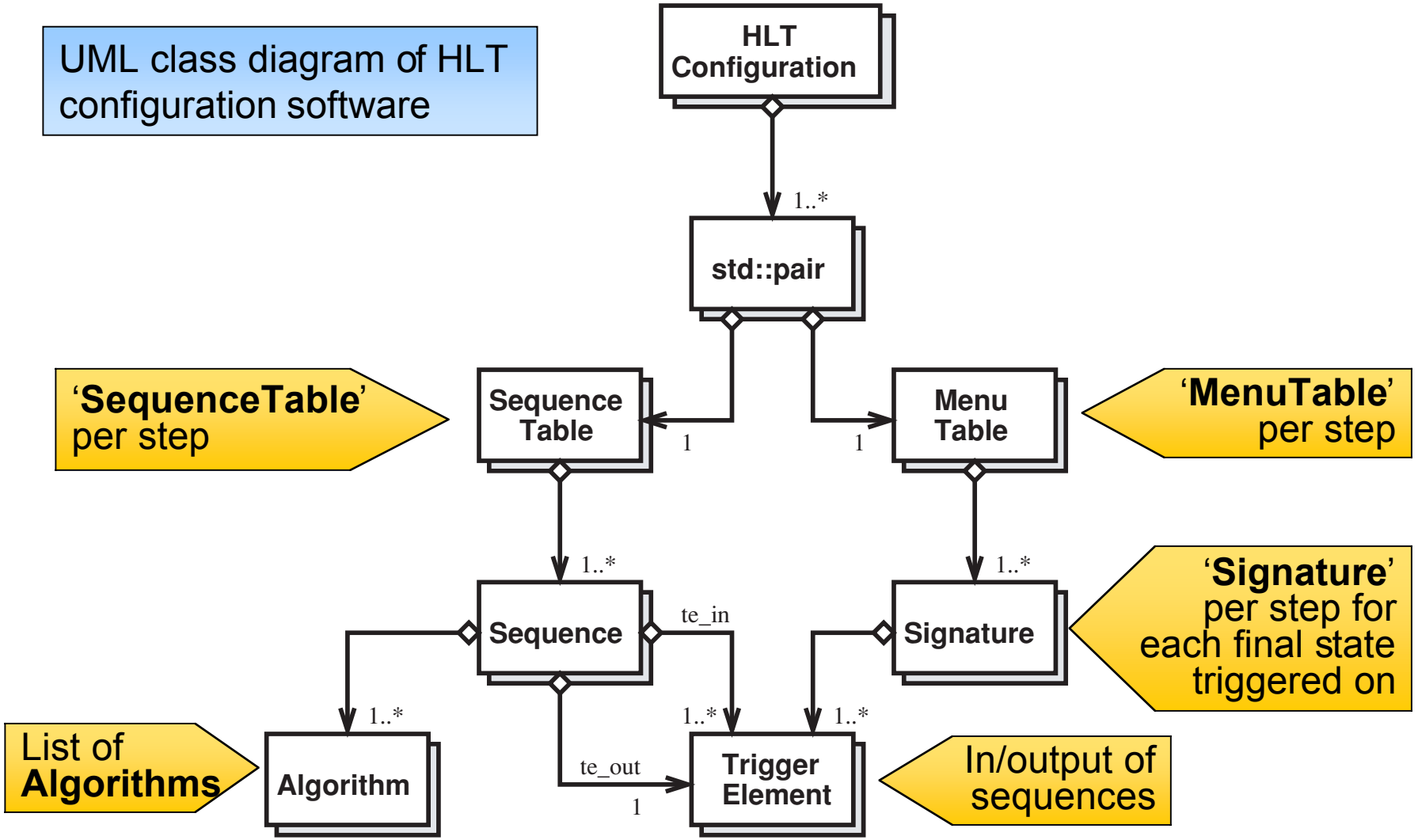
HLT: CONFIGURATION

Recursively 'top-down':
- *Input 1*: final/physics **Signature** '2e30i'
- *Input 2*: all known **Sequences** (Algorithms+In/Outputs)



HLT CONFIGURATION: REALISATION

XML for Sequences + physics Signatures
Embedded in HLT-SSW and Atlas offline framework Athena



SUMMARY

Multi-layer structure of trigger for rate reduction 40 MHz → ~100 Hz
Separate configuration tasks for LVL1 and HLT

LVL1 Trigger

- Hardware-based trigger using calo / muon inputs
- LVL1 selection strategy defined using XML and C++
- Common configuration for hardware and simulation

HLT

- Software trigger seeded by LVL1
- 'fast rejection': - Regions-of-Interest
  - step-wise processing
- Consistent LVL2 and E.F. configuration
- Recursive algorithm to derive HLT steering

Future

- Common configuration for LVL1 and HLT
- Main issues: Consistency and efficiency!